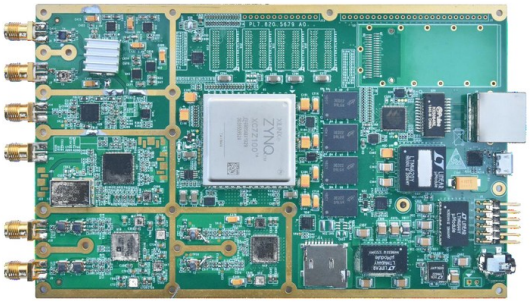
HPORTEK

PRODUCT DATASHEET

SYHS-DRFM

High-Speed Acquisition & Generation Board

The SYHS-DRFM is a general-purpose high-speed acquisition and generation platform integrating one dual-channel high-speed DAC, one dual-channel low- speed ADC, and one dual-channel high-speed ADC, with multi-bus communication and control. Built around the ZYNQ processing core, it performs filtering, channelization, and decimation. The PS side has 1 GB memory and the PL side 2 GB, with UART, RS422, GPIO, and Ethernet interfaces reserved.



Features

• Integrated dual-channel acquisition circuits

• Integrated dual-channel high-speed DAC

• Abundant FPGA resources FPGA

• Large DDR3 memory

• Abundant bus interfaces

• External Clock Input

• JTAG for debugging & secondary development

Published technical information

Parameter	Specification / typical value
DAC Performance	
Output Frequency	Supports 9kHz to 6GHz
Resolution	16bit
Number of Channels	Independent dual-channel
Sampling Rate	Up to 12.6 GSPS (configurable)
SFDR	≤-83dBc@1.8G

Parameter	Specification / typical value
Output Signal Power	-10dBm @ 50Ω (fine adjustment available)
Number of Channels	2 channels
Coupling Mode	Ch.1 AC coupling; Ch.2 DC coupling
High-Speed ADC Performance	
Resolution	14bit
Sampling Rate	Up to 1.25 GSPS (configurable)
SNR	60dBFS@375MHz，1GSPS
SFDR	70dBFS@375MHz，1GSPS
Number of Channels	Independent dual-channel
ENOB	9.6bit
Analog Input (Ai)	1.46Vp-p≤Ai≤1.94Vp-p
Sampling Bandwidth	≤625MHz
Coupling Mode	AC coupling
Low-Speed ADC Performance	
Resolution	16bit
Sampling Rate	Up to 80 MSPS (optional)
SNR	77.6dBFS@7MHz
SFDR	93dB FS@7MHz
Number of Channels	Independent dual-channel
ENOB	12.6bit
Number of Channels	Independent dual-channel
Channel Isolation	93dBc
FPGA Performance	
Model	XC7Z100-2FFG900I
Processor	Dual-Core ARM Cortex-A9 MPCore Up to 1GHz
Logic Cells	444K
LUTs	277.4K
Block RAM	26.5Mb
DSP	2020

Parameter	Specification / typical value
Flip-Flops	554.8K
Memory	
DDR3	PS: 1GB at 1600MT/s; PL: 2GB at 1600MT/s
SD Card	32GB default
Dual QSPI Flash	2*256Mbit
Communication	
QSFP: 40Gbps data rate	Supported
USB debug serial port	Supported
General GPIO ports	Supported
Input Clock Frequency	100MHz (internal or external, selectable)
Signal Formats	Built-in AM, FM, CW, FMCW (others to be developed)
General	
Power Supply	+12V DC / ≤2.5A (full operation)
Dimensions (L×W×H)	181 mm × 100 mm × 38.3 mm (with heat sink)
Weight	≤680g

Prepared from the existing product catalogue. Specifications may change; typical values are not guaranteed limits. Confirm operating conditions, interfaces and ordering configuration with engineering. This document does not replace the equipment operating manual.

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https://www.hportek.com/en/product/high-speed-acquisition-board-syhs-drfm/